In the claims:

Following is a complete set of claims as amended with this Response.

1. (Currently Amended) An apparatus comprising:

a logic structure integrated in an integrated circuit (IC), the logic structure having a set of bus inputs to generate events, a mask register to select inputs from among the set of bus inputs, a logic register to select logic to apply to the selected inputs and an event output to supply the result of the applied logic; ~~and~~

a bus interface integrated in the IC and coupled to the logic structure to transmit settable parameters to the mask register and the logic register of the logic structure from an external agent

a debug bus coupled to the bus inputs;

a test mode unit coupled to the debug bus;

node observation architecture logic to interface with the debug bus and control events generated by the logic structure; and

external pins coupled to an external pin observation block for communication with the external agent through the test mode unit.

2. (Original) The apparatus of Claim 1, wherein the logic register comprises a delay register to apply selected delays to the selected inputs.

3. (Original) The apparatus of Claim 1, wherein the logic register comprises a compare register to set compare functions to apply to the selected inputs.

4-6. (Canceled)

7. (Original) The apparatus of Claim 1, further comprising a configuration bus for receiving the settable parameters from the external agent and providing them to the logic structure.

8. (Original) The apparatus of Claim 1, wherein the bus interface allows the event output to be read by the external agent.

9. (Original) The apparatus of Claim 1, wherein the logic structure further generates a system management interrupt based on the event output.

10. (Currently Amended) An apparatus comprising:

a counter register integrated in an integrated circuit (IC) and coupled with an external unit integrated in the IC to receive results of operations from the external unit;

a logic structure integrated in the IC to receive signals from the external unit, to send operations to the external unit, to generate events based on the received external signals and received settable parameters, and to send the events to the counter register to affect the operation of the counter register[[;]] , the logic structure having a comparator to produce comparisons using the signals received from the external unit; and

a bus interface integrated in the IC and coupled to the logic structure to transmit settable parameters to the logic structure from an external agent.

11. (Canceled).

12. (Currently Amended) The apparatus of Claim 10 ~~Claim 18~~, further comprising a mask register coupled to the bus interface and to the logic structure, the mask register receiving settable values from the bus interface, the settable values selecting portions of the signals received from the external unit.

13. (Previously Presented) The apparatus of Claim 10, further comprising a delay register coupled to the bus interface and the logic structure to select delays for portions of the signals received from the external unit.

14. (Currently Amended) The apparatus of Claim 10 ~~Claim 11~~, further comprising a compare register coupled to the bus interface and the comparator to select a compare functions to be executed by the comparator.

15. (Original) The apparatus of Claim 10, further comprising a clock source register coupled to the logic structure to select a clock source of the IC for use by the logic structure.

16. (Original) The apparatus of Claim 10, wherein the bus interface further allows the counter register to be read by the external agent.

17. (Original) The apparatus of Claim 10, wherein the counter register further generates an interrupt based on results of operations form the external unit.

18. (Currently Amended) A method comprising:

receiving settable ~~of~~ parameters in a logic structure of an integrated circuit (IC) from an external agent integrated in the IC through a bus interface integrated in the IC and coupled to the logic structure;

receiving signals in the logic structure from an external unit integrated in the IC;

sending operations from the logic structure to the external unit;

receiving results of operations performed by the external unit in a counter structure of the IC;

~~receiving a set of bus inputs in the logic structure of the IC;~~

applying logic to the received signals and received settable parameters ~~selected bus inputs~~ in the logic structure to generate an event using a comparator to produce comparisons using the signals received from the external unit; and

applying the events to the ~~to a~~ counter structure.

19. (Currently Amended) The method of Claim 18, further comprising providing the events over a bus to the ~~to an~~ external agent.

20. (Original) The method of Claim 18, further comprising generating an interrupt based on the event.

21. (Original) The method of Claim 18, further comprising applying selected delays to the selected inputs based on the received settable parameters.

22. (Currently Amended) The method of Claim 18, wherein using a comparator comprises ~~further comprising~~ applying compare functions to the selected inputs based on the received settable parameters.

23. (Original) The method of Claim 18, further comprising applying a mask in the logic structure to select inputs from among the bus inputs.

24. (Currently Amended) A method comprising:

receiving settable ~~of~~ parameters in a logic structure of an integrated circuit (IC) from an external agent;

receiving a set of bus inputs in the logic structure of the IC;

selecting inputs from among the set of bus inputs based on the settable parameters using a mask register of the logic structure;

applying logic to the selected bus inputs in the logic structure to generate an event the logic being selected based on the settable parameters; ~~and~~

generating a system management interrupt based on the event

controlling events generated by the logic structure using node observation architecture logic to interface with a debug bus coupled to the bus inputs and a test mode unit coupled to the debug bus; and

communicating with the external agent through the test mode unit using external pins coupled to an external pin observation block of the observation architecture logic.

25. (Currently Amended) The method of Claim 24, wherein communicating comprises ~~further comprising~~ providing the events over a bus to an external agent.

26. (Original) The method of Claim 24, further comprising applying selected delays to the selected inputs based on the received settable parameters.

27. (Original) The method of Claim 24, further comprising applying compare functions to the selected inputs based on the received settable parameters.

28. (Currently Amended) The method of Claim 24, wherein selecting inputs comprises ~~further comprising~~ applying a mask in the logic structure to select inputs from among the bus inputs.

29-32. (Cancelled)